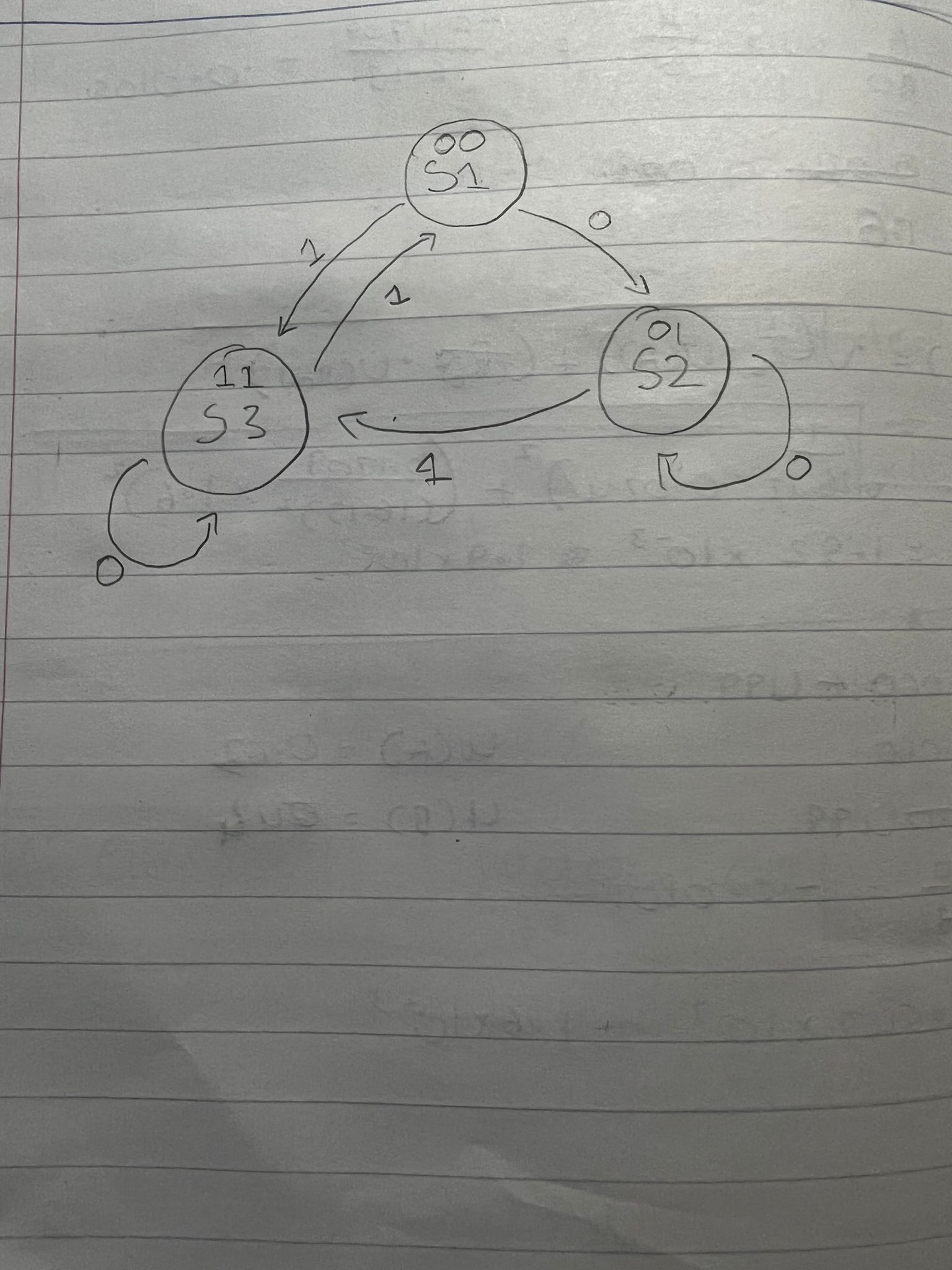
**Exercise 3**

**State Diagram:**

First, we make a state diagram to get better understanding of our states to make transition state table later on.

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**State Table:**

We will be using the D-Flip Flops to hold the bits for our states, D-flipflops have only one input and their input depends on the previous one.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Present  State | Input | Next  State | D1 | D2 | Output |
| S1 | 00 | 0  1 | 01  11 | 0  1 | 1  1 | 0  0 |
| S2 | 01 | 0  1 | 01  11 | 0  1 | 1  1 | 1  0 |
| S3 | 11 | 0  1 | 11  00 | 1  0 | 1  0 | 0  1 |

**Karnaugh Map:**

Now we make the Karnaugh Map for D1 and D2 to find the functions to make our circuit.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BX | | | | | |
| A |  | ***00*** | ***01*** | ***11*** | ***10*** |
| ***0*** | 0 | 0 | 1 | 0 |
| ***1*** | 1 | 1 | 0 | 0 |

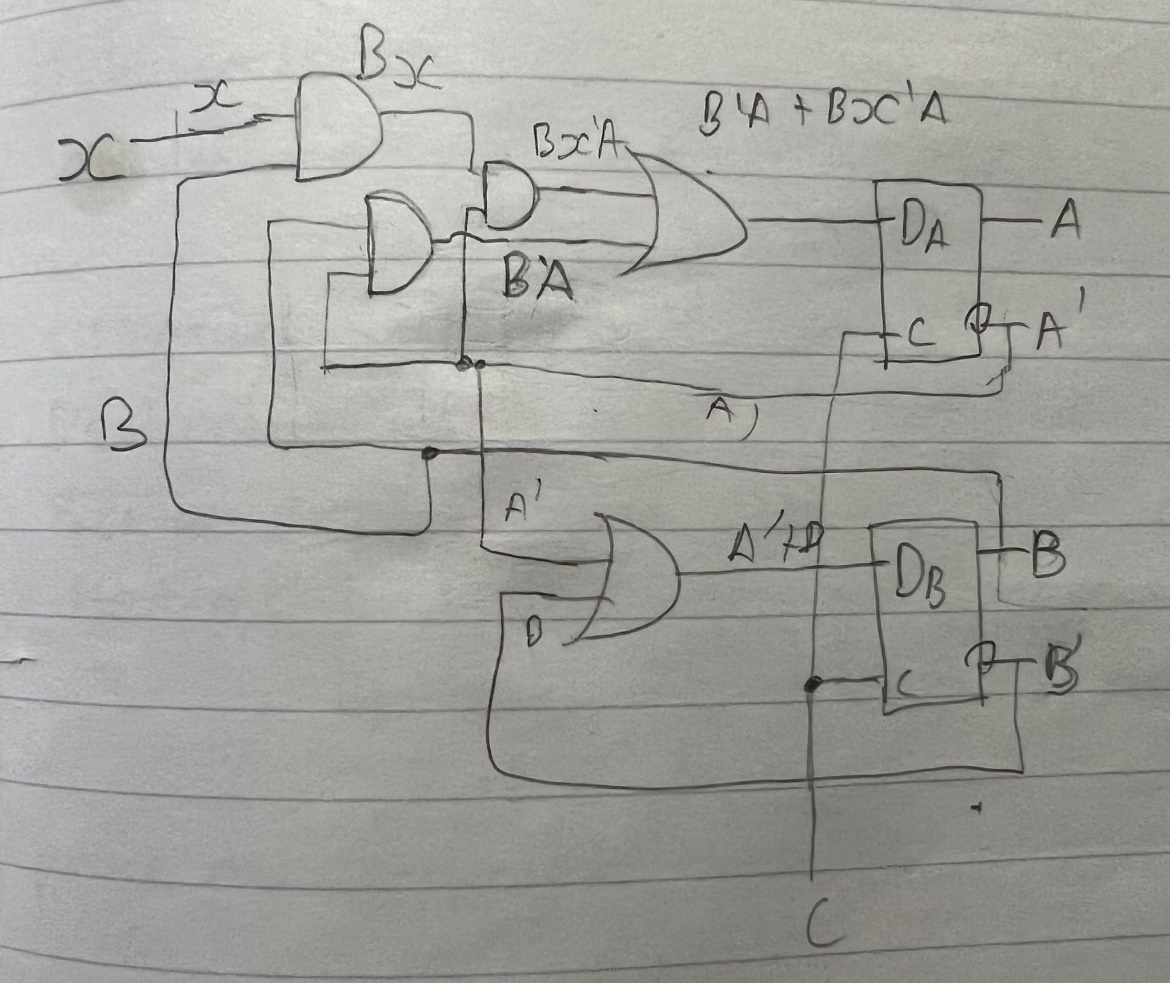
D1 = B~A +BX~A

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BX | | | | | |
| A |  | ***00*** | ***01*** | ***11*** | ***10*** |
| ***0*** | 1 | 1 | 1 | 0 |
| ***1*** | 1 | 1 | 0 | 0 |

D2 = ~A + B

**Circuit (OR, AND, NOT):**

Here we create the circuit using AND and OR gates and 2 D-Flipflops

****

**Conversion of Circuit(NAND ONLY):**

Now we use the conversion rules for AND,OR gate to NAND gates to make the final NAND gate circuit only.

Diagram

Description automatically generated

Now we cancel the invertors that are in the same rule because ~a~a=a

Diagram, schematic

Description automatically generated

**Conclusion:**

We started off with creating a diagram to get a better understanding of the states, we then used that diagram to make the state transition table to get our values for D1 and D2 so we can make the excitation table for D1 and D2 to get the functions(D1 = B~A +BX~A , D2 = ~A + B) that we require to create a sequential circuit using 2 D-flip flops and AND,OR gates then we convert the gates to invertors and Nand gates and cancel the ones in the same row to get our final NAND sequential circuit.